A 1.9-GHz GaAs Chip Set for the Personal Handyphone System

Finbarr McGrath, Karen Jackson, Eugene Heaney, Allan Douglas, William Fahey, Russell G. Pratt, and Ted Begnoche

Abstract—**The Japanese Personal Handyphone System (PHS) is representative of the latest generation of digital portable communications systems currently being deployed. Enabling technologies for these systems include high performance Radio Frequency Integrated Circuit (RFIC) chip sets. These chip sets allow all the RF transceiver functions to be included in low cost surface mount plastic packages. With the addition of filters and bypassing capacitors, the RF portion of the phone shares the same printed circuit board (PCB) as the DSP, CODEC, and Logic IC's. The availability of such highly integrated 1.9-GHz RFIC's requires the solution of many complex design, manufacturing, and test problems. This paper explains the critical issues relating to the air interface of the PHS system and how it affects the RFIC design. The chip partition, design, and performance of each subfunction is discussed relative to the requirements imposed by the air interface. The result is a highly integrated, cost effective solution that occupies the minimum board area.**

I. Introduction

THE PERSONAL Handyphone System defined by Japan's Research and Development Center for Radio System (RCR) establishes the minimum requirements for the unified digital mobile telephone system. The standards defined in document #28 (RCR-28) cover the communications control methods, protocols, encryption, voice coding, and air interface [1]. The document also serves as a guideline for private systems based on the publicly established minimum requirements. The concept behind the Personal Handyphone System is to provide a low data rate, digital, two-way wireless link from any hand-held terminal at any time or place. The hand-held terminal is pocket sized and similar in weight and appearance to the smallest cellular phones. The RCR-28 standard ensures that any hand-held terminal can provide common access to home, office, and public (outdoor) locations in the coverage area. While the original concept was designed around a voice system, its digital nature makes paging, low data-rate video, fax modem, data communication, and ISDN applications possible. The standard is flexible enough to make provision for private wireless branch exchanges (WPABX), peer to peer communications or home cordless phones coexisting with the public digital cordless phone system. Thus the hand-held unit can be used in the home as a cordless phone, in the office as part of a PABX system or in the street as part of the public PHS network. Only one phone number is required. The public network provides for many of the features of cellular systems such as roaming and hand-off. The interoperability ensured by RCR-28 will allow major telephone systems operators such as Nippon Telephone and Telegraph (NTT) to coexist with manufacturers of portable consumer electronics, such as Sony Corp. Once the public infrastructure is complete the growth is expected to be explosive.

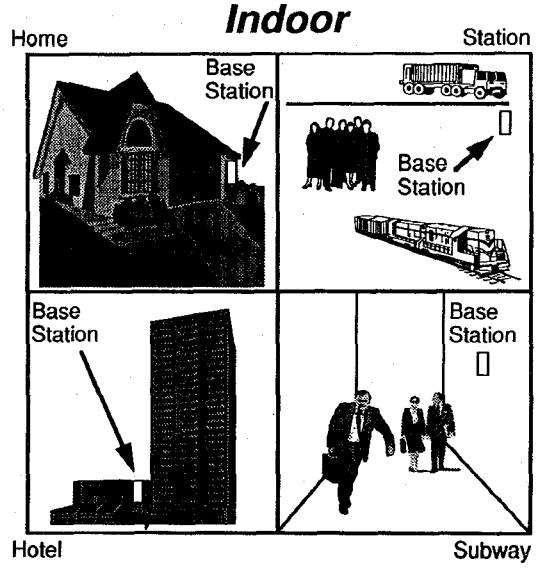

Fig. 1. PHS system concept.

Fig. 1 shows the PHS system concept. It is essentially a microcellular system with cell sites of approximately 50-m radius. The base stations are placed on telephone poles at regular intervals in the street or private units can be purchased for the home. The average transmit power varies from +19 to +27 dBm, depending on equipment classification, and is much less than a cellular base station. Hand-off is accomplished at a slow rate as the user walks from one cell site to the next. The system does not hand-off quickly enough to be used in vehicles. The access method is TDMA/FDMA utilizing 77 RF channels from 1895.15–1917.95 MHz. The channel spacing is 300 kHz but the minimum allowed spacing for two channels that are spatially collocated is 600 kHz. In any given frequency channel four voice channels are available using a TDMA/TDD protocol. The timing protocol is shown in Fig. 2 and uses a frame length of 5 mS with four time slots for both transmit and receive of 626-μS duration. The voice transfer rate is 32 kB/s using ADPCM.

Manuscript received June 30, 1994; revised February 20, 1995.

The authors are with the M/A-COM Microelectronics Division, Lowell, MA 01851 USA.

IEEE Log Number 9412079.

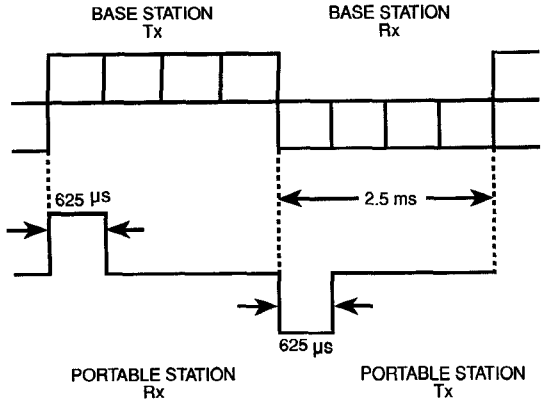

Fig. 2. Time division duplex in the PHS system.

As the system is intended at the outset for portable handheld applications power consumption is a premium. The main concern in developing the chip set was to implement the Air Interface standards in the most cost effective manner with minimum power consumption.

II. The Air Interface for PHS

The Air Interface specifies transmitter and receiver performance allowed in the RF channel. It defines the allowable modulation technique; the spectral content of the baseband signal; the filter transfer function; and allowed carrier frequencies. During transmit the air interface determines allowable transmit power levels and limits interference into adjacent channels (ACI) and spurious output. The transient response during duplexing or burst-mode is also specified. During receive the sensitivity is specified for a given bit error rate (BER) and receiver intermodulation immunity and selectivity is defined. The key specifications of the air interface are outlined in Table I. The on air data rate including ramp bits, preamble and error correction is 384 kB/s.

During a transmit burst the average transmit power at the antenna is +19 dBm (80 mW). Once a transmit burst is complete the leakage power should not exceed 80nW, implying 60-dB on/off ratio. The transmitter should switch on or off during burst mode in 13.0 μs (5 bits) in a monotonically increasing or decreasing fashion. The transmitter should not generate any spurious levels in the RF band (1895.15–1917.95 MHz) that exceed −36 dBm. The transmitter should not generate any out of band spurious that exceed −26 dBm. In practice the unwanted lower sideband or the local oscillator leakage are the largest spurious signal levels to be filtered out.

The modulation scheme required in PHS is $\pi/4$ DQPSK. In this scheme the binary data is combined in a serial to parallel converter and differential coder to generate the impulses I_K and Q_K. The low pass filter $H(f)$ generates shaped pulses in the time domain $i(t)$ and $q(t)$, which are modulated by a single sideband modulator. This results in differentially encoded phase shifts $\Delta\Phi$ as shown in Fig. 3. While there are eight phase states possible in this scheme, only four can be chosen at any given phase transition yielding 2 bits/symbol (Fig. 4). The low pass filter $H(f)$ determines the occupied bandwidth of the system. It also determines instantaneous amplitude and

TABLE I
PHS Air Interface Requirements

Parameter	Performance
Access method	TDMA/FDMA
RF Frequency (MHz)	1895.15 - 1917.95
Number of Channels	77
Channel Spacing (kHz)	300
Frequency Assignment	Dynamic
Duplex Method	TDD
Frame Length Tx/Rx (ms)	5
Number of slots/frame	4
Slot Duration (microseconds)	625
Bit Time (microseconds)	2.6
Transfer Rate (kb/s)	384
Tx Power peak//avg (mW)	80/10
Power Control (dB)	20/40
Modulation	$\pi/4$ DQPSK (α = 0.5)
ACI in 192kHz Band @ 600kHz Offset (dBc)	51
Spurious Output (dBm)	-26
Sensitivity @ BER = 1% (dBm)	-100
Intermodulation Immunity @ -97dBm and BER = 1% (dBc)	47
Circuit Modes	Tx/Rx/Sleep

phase during phase transitions. The filter transfer function (root Nyquist) is defined for

$$H(f) = 1 \quad \text{for } 0 \le |f| < \left(\frac{1-\alpha}{2T}\right)$$

$$H(f) = \cos\left[\frac{T}{4\alpha}\left(2\pi|f| - \frac{\pi(1-\alpha)}{T}\right)\right] \quad \text{for} \left(\frac{1-\alpha}{2T}\right) \le |f| < \frac{1+\alpha}{2T}$$

$$= 0 \quad \text{for} \frac{1+\alpha}{2T} \le |f|$$

where T is the bit rate and $\alpha = 0.5$. This filter transfer function has a high spectral efficiency since the power density drops to zero at 1.5 times the ideal Nyquist rate. In practice this baseband filter is implemented digitally. The major disadvantage of this filter function is that the resulting filtered signal is not constant envelope. In fact is will vary from +2.9 to −11 dB about the power level at the sampling points. If the transmit chain is perfectly linear then the RF spectrum at 1.9 GHz is a perfect double sideband representation of the baseband signal. However, any transmit chain nonlinearity in amplitude or phase will generate side lobes outside the ideal Root Nyquist filter bandwidth. In this case the baseband filter no longer determines the occupied bandwidth. As the nonlinearities become more extreme, power can spread into adjacent channels at 600- and 900-kHz offset. Since this can seriously disrupt communications in other bands the system specifies the maximum allowed adjacent channel power to be −31 dBm @ 600 kHz and −36 dBm @ 900 kHz from the carrier. For +19 dBm transmit power translates to 50 and 55 dBc of adjacent channel leakage suppression. In order to achieve optimum power added efficiency (PAE) it is desirable

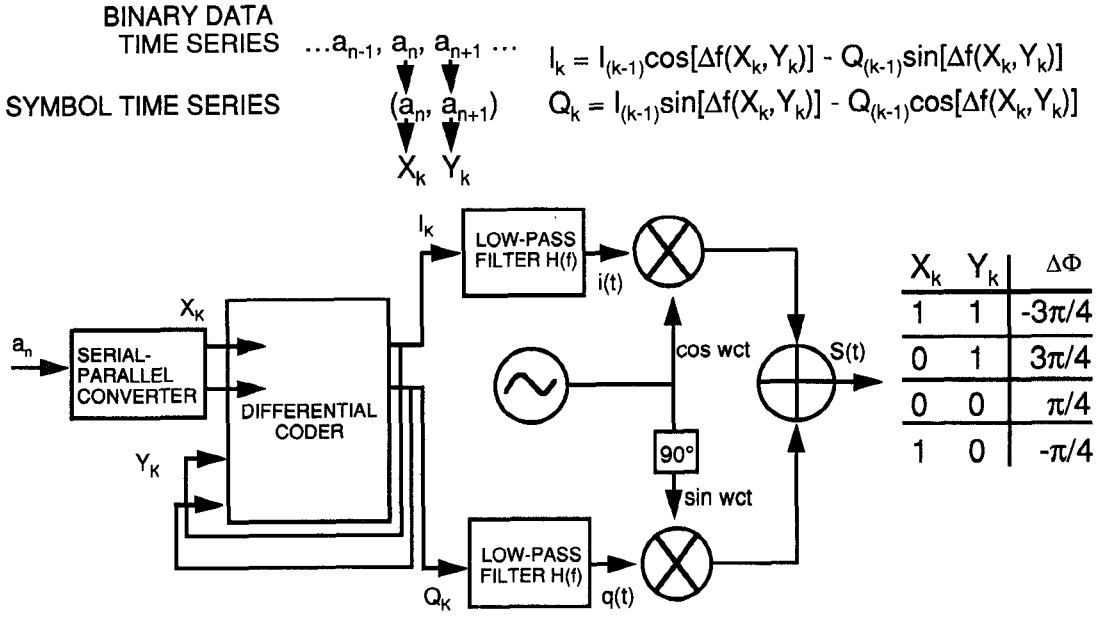

Fig. 3. $\pi/4$ DQPSK phase encoding.

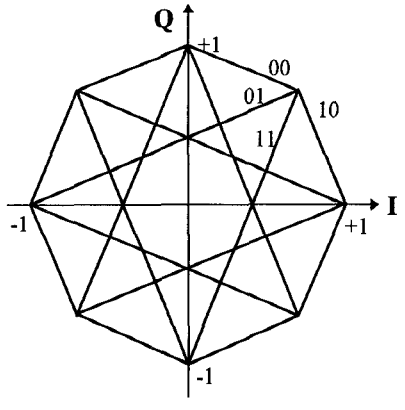

Fig. 4. $\pi/4$ DQPSK I—Q diagram.

to operate the power amplifier at the highest RF power level possible. The major design trade off in the Tx chain is between linearity and power added efficiency. As the transmit chain is compressed the maximum and minimum deviation from the ideal will vary. The system allows for +1.1 and −3 dB margin and the instantaneous power during each transmission burst is defined by Fig. 5.

The low noise amplifier, Rx Filter, and first down converting mixer determines the receiver sensitivity and intermodulation immunity of the overall receiver. In the RCR-28 document the sensitivity is defined to be less than −97 dBm when the BER = 1%. Another key receiver specification is the sensitivity in the presence of two strong interfering signals. With a reference signal set at −94 dBm and two strong interferers detuned at 600 and 1200 kHz from the reference signal the interfering signals should be at least 47 dB above the reference level when the BER drops to 1%. Fig. 6 defines these specifications graphically. If the phone is "on the hook" but not actively receiving data the receiver is switched on every 100 mS to synchronize in time and frequency with the local base station and detect any incoming calls. Thus the receiver demand on the battery is much higher than the transmitter. Receiver current consumption needs to be minimized.

III. Chip Set Design Considerations

Given the requirements defined by RCR-28 the chip set design considerations can be grouped into four interrelated categories:

1) Factors affecting the Transmit chain
2) Factors affecting the Receive chain
3) Electromechanical considerations
4) System timing and operating modes

A. Transmit Chain

The main goals in the Transmit chain are to meet transmit power levels and linearity, filter unwanted spurious outputs, and optimize power added efficiency. Assuming that the transmit power amplifier design can achieve 20 dB or more gain, then power added efficiency is optimized by allowing the power amplifier to operate at the highest level of nonlinearity consistent with the ACI specification. The rest of the transmit chain is designed to operate linearly. The difference between nominal Tx power and allowed out of band spurious determines the degree of filtering. In this case

$$P_{\text{out}} - P_{\text{spurious}} = 19\ \text{dBm} - (-26\ \text{dBm}) = 45\ \text{dB}.$$

At typical IF frequencies of 90 or 240 MHz there is little selectivity in the upconverter. Thus all of the filtering must come from external filters distributed in the Tx chain. The overall level of filtering needs to be as high as 55 dB for production margin. This fact precludes putting the entire transmit chain in a single package since package isolations of 55 dB are not easily achieved. A convenient break in the

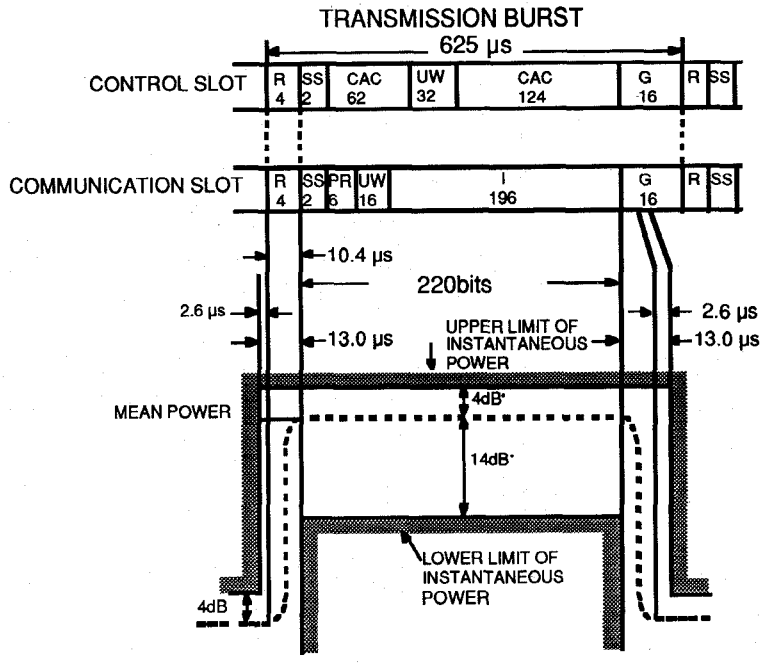

Fig. 5. PHS transmission burst.

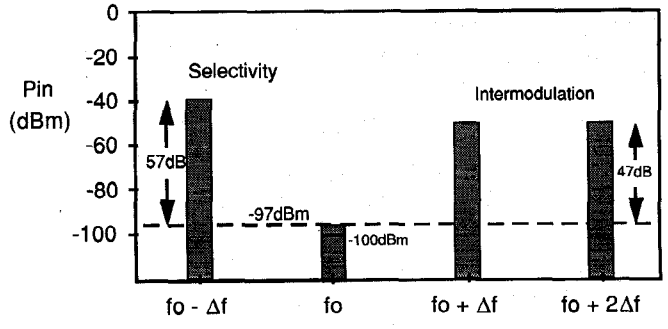

Fig. 6. Receiver specifications.

transmit chain must be found. Filtering the LO signal can be made easier by using a balanced mixer topology.

B. Receive Chain

The main challenge in the receiver design was to achieve the required sensitivity, intermodulation, and spurious rejection while operating at low supply voltage and current. The statistical nature of a digital receiver causes an increase in bit error rate (BER) as the ratio of received signal power to noise power decreases. The RCR specification requires the BER $>10^{-2}$ when -97 dBm of signal power is received. For $\pi/4$ DQPSK signal the ratio S_o/N_o should be 12 dB when the bit error rate is 10^{-2}. Thus the equivalent input noise floor is -97 dBm - 12 dBm $= -109$ dBm for the receiver.

As

$$N_o = \mathrm{kTBNF}$$
$$B = 225\ \mathrm{kHz}$$

the resulting noise figure is NF = 11.5 dB. With filter and PCB loss the noise figure required of the LNA downconverter is 9 dB. As with any multi-channel receiver, the intermodulation of signals in adjacent channels causes noise to be generated in the desired channel. This effectively reduces the carrier to noise ratio. The specification requires the system to have a BER better than 10^{-2} with -94 dBm of received power in the presence of two strong interfering signals offset at 600 kHz and 1.2 MHz. In this case there is thermal noise and intermodulation products in the received channel. We have

$$12\ \mathrm{dB} > \frac{S^o}{N_o + I}$$

assumed that the interference is essentially noise like. Thus

$$\frac{So}{I} > 15\ \mathrm{dB}$$

and the maximum intermodulation product is (-94 - 15) dBm $= -109$ dBm. The strong interfering levels are defined to be no less than -47 dBm. Therefore the minimum input intercept point is

$$\mathrm{IIP3} = P_{\mathrm{in}} + \mathrm{IMR}/2 = -47 + (-47 + 109)/2$$
$$= -16\ \mathrm{dBm}$$

C. Electromechanical Considerations

In keeping with the portable nature of the application it is desirable to keep the overall PCB area to a minimum. If the chip set is to be user friendly and truly a mass production product it has to be manufactured with high volume packaging and assembly technology. In this case a fine pitch shrink small outline (SSOP) 28 lead package is chosen. The high pin count, 25-mil lead pitch, and small size (150 × 390 mils) minimize the area required. The complete assembly and packaging in high volume cost 50–75 cents. The package lead widths are 14 mils, which make for conveniently narrow 50-ohm traces

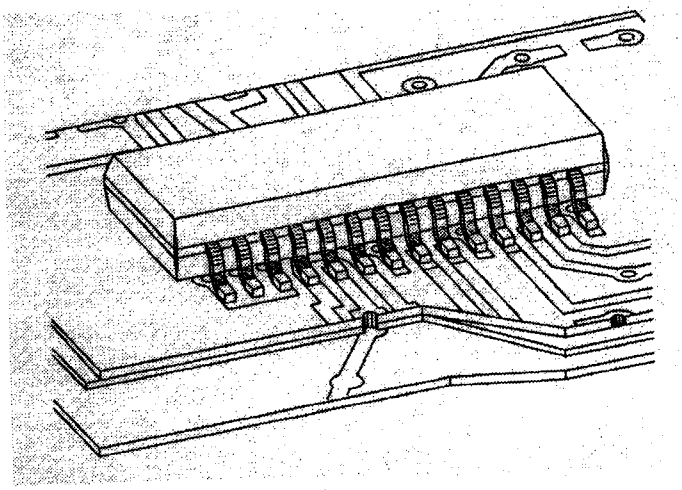

Fig. 7. SSOP 28 lead package on 4-layer FR-4 board.

on multi-layer PCB's. The disadvantage of this package is its lack of a solid ground since any RF grounding must be done through the leads. This causes potential for unwanted coupling between various functions and potential oscillation. It is necessary to model the complete IC in this chip for optimum results. The package also has significant electrical parasitics at 2 GHz with lead inductances from 1–2.5 nH and coupling capacitance from 60–100 fF. All these package and PCB parasitics must be absorbed into the design. Fig. 7 shows the SSOP 28 lead package mounted on a four layer PCB. The potential for unwanted coupling can clearly be seen.

D. System Timing and Operating Modes

A chip set that consumes less power ultimately allows for longer talk time between recharging or lighter weight batteries. As digital IC's move towards 3-V logic levels the pressure to make RFIC's meet performance goals at 3 V is increasing. As supply voltage drops the natural tendency is to increase current. No measure is spared to minimize power consumption. The TDMA/TDD nature of the system means that either the Transmit or Receive chain can be powered down when the phone is not transmitting or receiving. For each handset the transmitter or receiver is active for only 625 μs out of 5 ms, so powering down results in substantial savings. Also when the receiver is not active it only needs to poll the system at a very low duty cycle. Each chip must be designed with the facility to power down under control of the system timing logic.

Since one of the heaviest components in the portable radio is the battery every effort is made to make the entire system operate from the lowest battery voltage available. In practice such systems will operate from 3.6-V nominal supply voltage or 3.0 V regulated from the 3.6-V supply. We will now discuss the IC designs in detail.

IV. QPSK Modulator IC

The vector I/Q modulator is the interface between the digitally shaped $i(t)$ and $q(t)$ pulses at baseband of Fig. 3 and the RF carrier $s(t)$. Theoretically it is possible to convert from baseband to RF (1900 MHz). This requires a continuous-wave carrier signal at 1900 MHz, which can leak into the

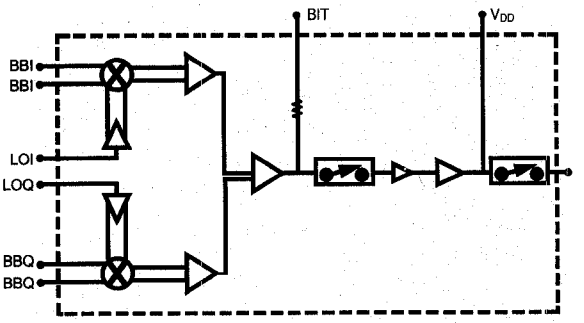

Fig. 8. QPSK modulator IC block diagram.

modulated RF channel. In practice it is impossible to isolate this carrier since 35–40-dB isolation is required. An IF of 90–240 MHz is typically chosen. The modulator should allow the predetermined phase encoded pulses $i(t)$ and $q(t)$ to linearly modulate the carrier according to

$$s(t) = a(t)\cos(\omega_c t - \phi(t))$$
$$a(t) = \sqrt{i^2(C) + q^2(t)}$$
$$\phi(t) = \tan^{-1}\frac{q(t)}{i(t)}$$

Fig. 8 shows the block diagram of the QPSK IC. Quadrature carrier inputs are provided to the chip along with differential in phase and quadrature baseband inputs

$$i(t), \overline{i(t)}, q(t), \overline{q(t)}.$$

The carrier inputs are amplified and split to provide complimentary drive to the mixers, which then upconvert the baseband data to 90 or 240 MHz. The output of each mixer is differential and is recombined with two amplifier stages, where their single ended outputs are then combined with another amplifier stage, thereby cancelling one of the sidebands. Perfect cancellation occurs when 0° phase and 0-dB amplitude imbalance is obtained. To that end, careful attention was made to the IC layout symmetry and biasing schemes. Both LO baluns and IF combiners as well as the I/Q combiner are realized using differential amplifiers. In order to ensure the best amplitude tracking on I and Q channels one current source is used for both the IF combiners and I/Q combiner.

A FET quad topology was used for the mixer designs. Each mixer contributes to the carrier leakage and therefore careful attention must be paid to the baseband drive and biasing. Single-ended baseband drive to the mixers is possible, although differential drive results in much better carrier suppression. In the PHS system, it is necessary to dc couple the baseband inputs, and on this IC each mixer was designed for inputs equal to 2.0 V. Because dc offset equates to excess carrier leakage, it is critical to maintain less than 5 mV offset across each mixer.

The 70 dB isolation requirement is obtained using two SPST switches. Complimentary control lines of 0 V and −4 V for each switch can be tied together externally or controlled independently. The switches are designed using series and shunt depletion mode FETs whose pinch off voltage is half that of the negative rail (−2.0 V), allowing a smooth, monotonic attenuation between the series and shunt devices.

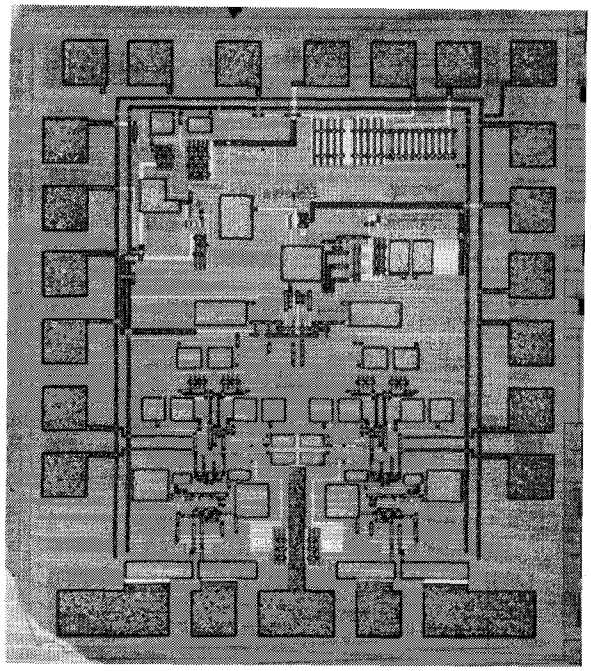

Fig. 9. QPSK modulator chip.

TABLE II
QPSK MODULATOR IC PERFORMANCE SUMMARY

Carrier Inputs LOI, LOQ	90 to 250 MHz -4 dBm
Baseband Inputs I, $\overline{I}$R, Q, $\overline{Q}$R	150 mV p-p 2.000V DC
VDD	+4 V
I(VDD) Tx Mode	18 mA
I(VDD) Save Mode	0.8mA
IF Pout, SSB	-7 dBm
Carrier Suppression	>30 dBc
LSB Suppression	>32 dBc
Burst Isolation	>75 dB
ACI (adjacent channel distortion)	>60 dBc at 600 kHz >40 dBc at 300 kHz

A two-stage common source network is used for the IF amplifier design where the output impedance of the second stage is transformed to 50 Ω using an external LC network. In this way, good distortion performance can be obtained with low power consumption.

Finally, the full integration is achieved on a single die design only 2.1 mm^2 in size, shown in Fig. 9.

The electrical performance and required inputs are summarized in the Table II. The IC is designed to operate from a +4-V supply and consumes only 72 mW of power. In order to save the battery life, the chip can be powered down using a negative logic pin and will consume less than 4 mW of power in this state.

The typical SSB output power is −7 dBm and varies less than 2 dB over temperature as shown in Fig. 10.

Fig. 11 shows the carrier and LSB suppression over the temperature range of interest. As is indicated, both these parameters are very stable over temperature. The resulting

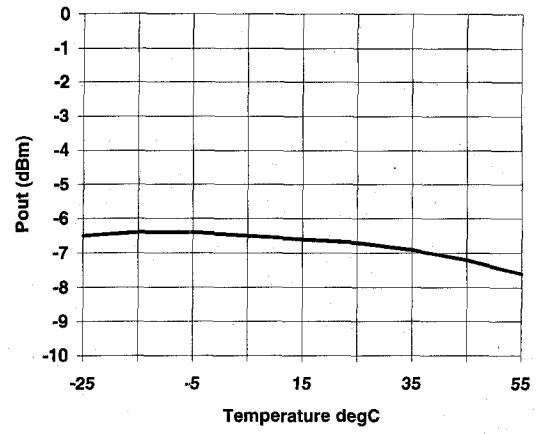

Fig. 10. Output power of modulator over temperature.

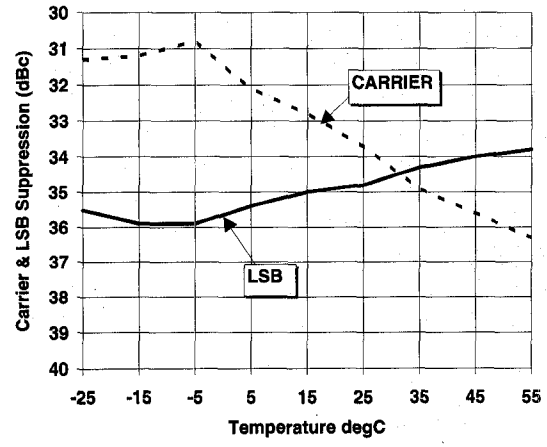

Fig. 11. Carrier suppression and LSB suppression over temperature.

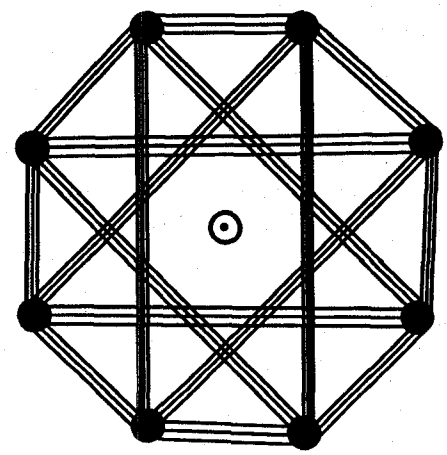

Fig. 12. RMS vector error of modulator.

RMS vector error plot is shown in Fig. 12. This plot includes the error generated by the baseband circuitry, which is roughly 2% resulting in a vector error for this design of 2.81%, significantly better than was budgeted.

Fig. 13 indicated the carrier leakage sensitivity to the dc offsets introduced at the baseband inputs. In order to maintain

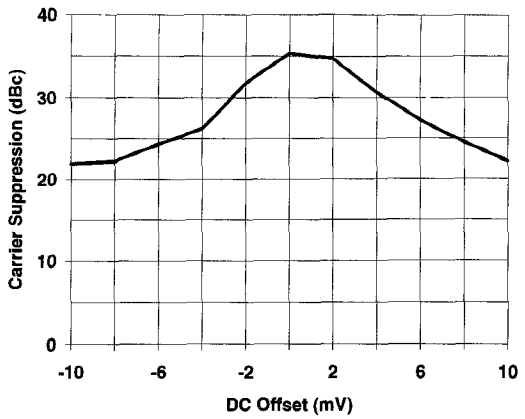

Fig. 13. Carrier leakage sensitivity to dc offsets.

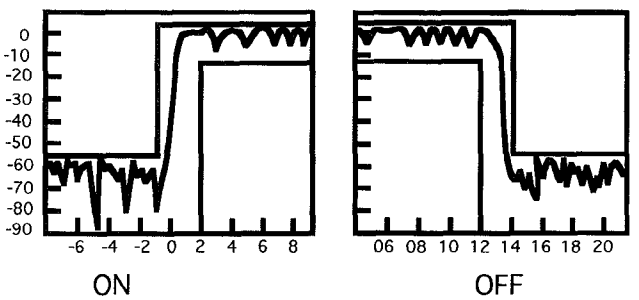

Fig. 14. Burst timing of QPSK modulator on/off.

an acceptable RMS vector error, carrier leakage should be better than 25 dBc resulting in a 5 mV allowable dc offset.

The burst timing sequence in Fig. 14 shows greater than 60 dBc on/off ratio achieved in a ramp up or ramp down time of less than 13.0 μS (2 symbols). There is no overlap into an adjacent time slot.

Using a PN9-drive at the baseband inputs, the output spectrum is shown in Fig. 15. For average output power of -10 dBm, the design demonstrates excellent linearity achieving 61 dBc adjacent channel power at 600-kHz offset against a 50-dBc system specification.

V. Transceiver Integrated Circuit

The main requirement of the downconverter is to achieve good sensitivity and dynamic range with minimum current consumption. Using a 1μm ion-implanted E/D process with low knee voltage and low maximum channel current, a complete up/downconverter was developed. The E-FET features a threshold voltage of +150 mV and $I_{\max}$ of 40 mA/mm. The D-FET features a pinch-off voltage of -0.6 V with 60-mA/mm IDSS. Using these devices a Transceiver consisting of an LNA and active downconverter mixer can be realized together with an upconverter mixer driver amplifier and step attenuator. A LO amplifier and LO switch is also realized.

The LNA sets the receiver sensitivity. It should have a good noise figure and sufficient gain to mask the mixer noise figure. The gain should not be so high that the input intercept point is degraded. To this end a cascade configuration is chosen since the gain is not excessive and the device can be series biased to conserve current. Fig. 16 shows the

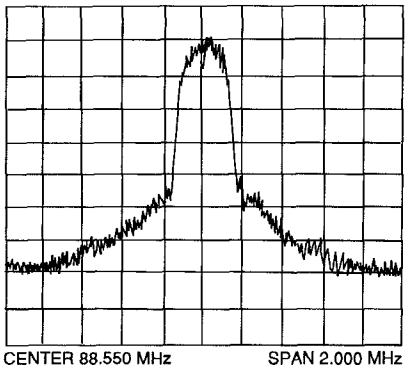

Fig. 15. Output spectrum of modulator with -7 dBm average power.

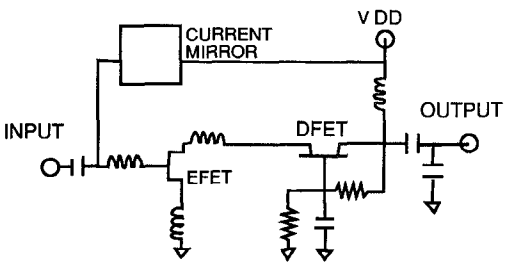

Fig. 16. LNA schematic.

LNA schematic. It utilizes inductive feedback to the common source E-FET to achieve simultaneous noise and impedance matching. Capacitive feedback is used in the common-gate device to optimize linearity, gain, and stability. The input impedance for the common source stage is approximated

$$Z_{\text{in}} = L_{gm}/C_{gs} + j\left(\omega L - \frac{1}{\omega C_{gs}}\right)$$

The inductance value

$$L = 50/2\pi \text{ ft}$$

where

$$\text{ft} = \frac{gm}{2\pi C_{gs}}$$

Using these equations L is selected to create a 50-ohm input real impedance. The E-FET is selected such that it provides sufficient gm to meet the required transducer gain. The key to optimizing the linearity of a low voltage cascode is to split RF voltage optimally between the FET's. By using capacitive feedback in the common gate stage the input impedance is increased by a factor of $(1 + C_{gs}/C)$. The RF voltage is dropped across the common gate input capacitance C_{gs} and the feedback capacitor C. This technique can be used to optimize the linearity. The LNA output is matched for transducer gain and linearity. The impedance transformation is provided by a single tuned LC circuit that presents a 350-Ω load impedance to the FET while matching the LNA output port to 50 ohms. The LNA achieves 13-dB gain and 2.6 dB noise figure at 3 V and 2 mA, which is equivalent to the best discrete or single function MMIC's currently available [2], [3]. The gain and noise figure also show less than 1 dB and 0.5-dB variation from -20 and 70°C. (Figs. 17 and 18).

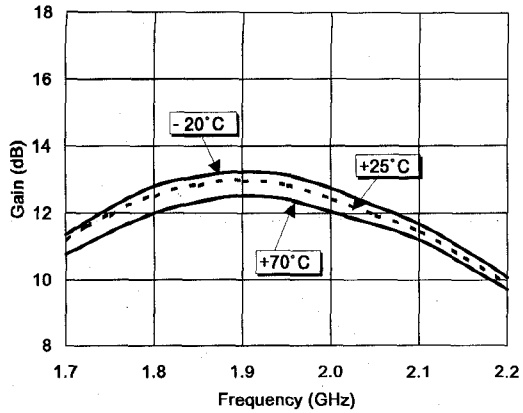

Fig. 17. LNA gain at 3 V and 2 mA.

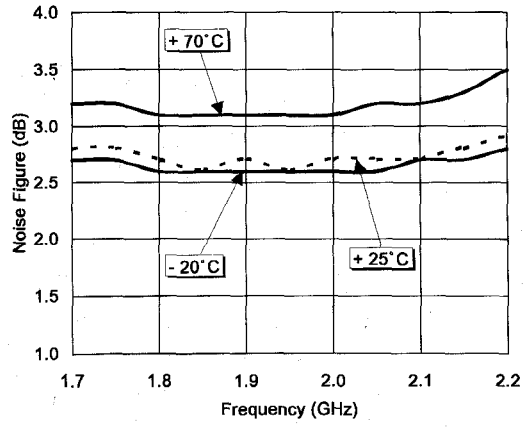

Fig. 18. LNA noise figure at 3 V and 2 mA.

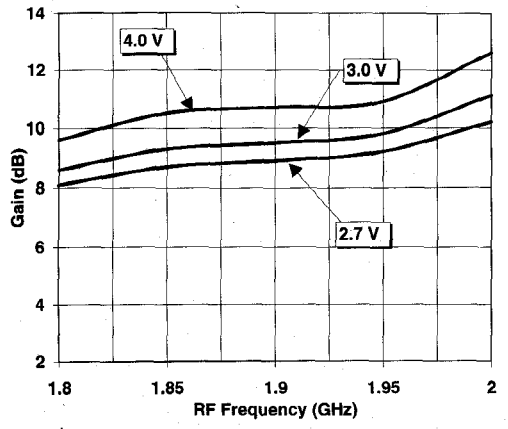

Fig. 19. Receive mixer conversion gain.

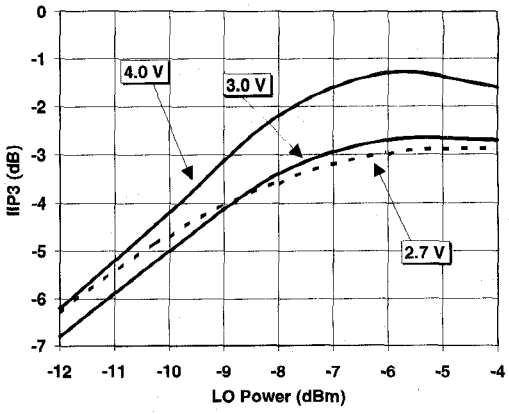

Fig. 20. Receive mixer third-order input intercept point.

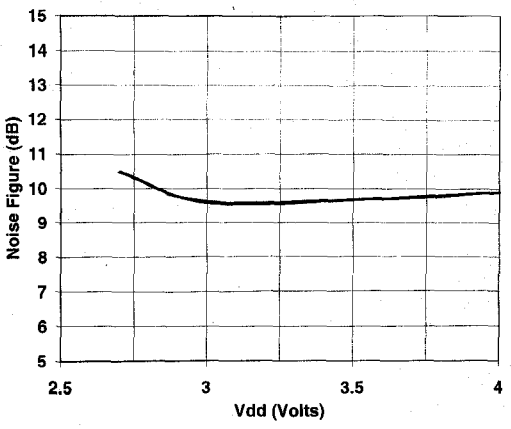

Fig. 21. Receive mixer SSB noise figure.

The receiver mixer is an active single-ended FET design. The LO and RF are summed into the gate of the mixing FET using current sources and a summing circuit. The gain of the LO and RF combiner allows low noise figure and low LO drive to be achieved simultaneously. The conversion gain at 2.7 V is 9 dB with an input intercept point of −4 dBm. The mixer noise figure is 9.5 dB. Figs. 19, 20, and 21 summarize the mixer performance.

The combined LNA and Receive Mixer assuming 2 dB loss in the receive image filter allows for an input intercept point of −14 dBm at the input to the LNA or −12 dBm at the antenna input. This allows 4-dB margin to be achieved against the system specification of −16 dBm. The receiver noise figure at the input to the LNA is 3.5 dB. Refering to the antenna input, the noise figure is 5.5 dB, which gives 6-dB production margin. This significantly increases the sensitivity of the radio over the minimum required by the system allowing for high yields in mass production. The entire receiver including LNA, receive mixer and LO buffer amplifier draws only 8 mA @ 3 V.

The main concept behind the transmit chain design is to allow reasonable levels of filtering and optimize the power added efficiency of the complete chain. Since the PA consumes most of the dc power it is optimal to drive the PA as hard as possible without degrading the adjacent channel interference (ACI) specification. Therefore all the other components in the chain must be linear in operation.

A key feature of the Transceiver is a linear transmit mixer, which is essentially a balanced Gilbert cell upconverter [4]. To maintain linearity and good LO suppression, it is necessary to operate the mixer at a level where the third order intermodulation ratio (IMR) is better than 40 dBc at the mixer output. In this case the output intercept point of the mixer is minimum of +6 dBm when operating with −14 dBm—output power. The intermodulation ratio is held at 40 dBc by this design. The LO leakage measured at the mixer output is better than

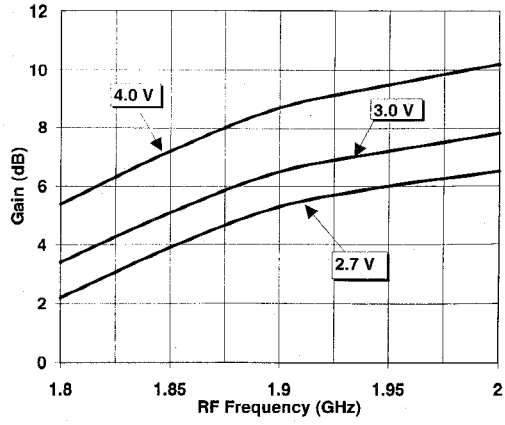

Fig. 22. Transmit mixer conversion gain.

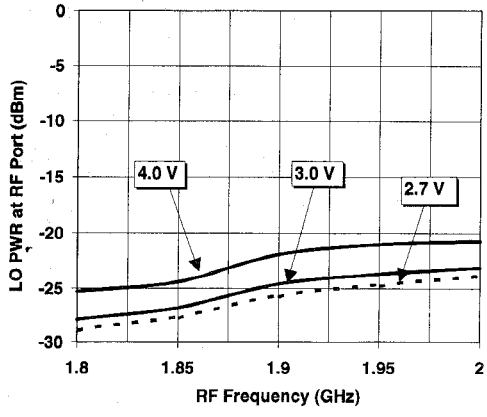

Fig. 23. Transmit mixer L_o leakage.

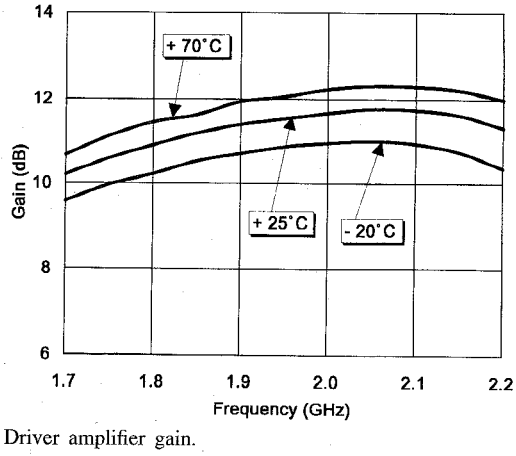

Fig. 24. Driver amplifier gain.

-20 dBm with -8 dBm of LO drive. Since the on chip LO amplifier supplies 8-dB gain the LO to RF isolation is better than 20 dB. Thus filtering of the LO is simplified. The mixer consumes 20 mA at $+3$ V. Figs. 22 and 23 show the mixer conversion gain and LO leakage.

Following the mixer in the Tx Chain is a driver amplifier with 11-dB gain drawing 10 mA of bias current. Fig. 24 shows the power gain of this amplifier. The amplifier is designed to deliver 0 dBm of drive to the power amplifier. As with the mixer and modulator the key design issue for the driver amplifier is linearity. The amplifier is driven with a $\pi/4$

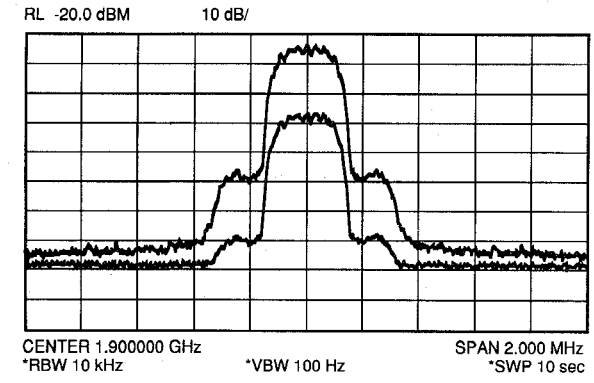

Fig. 25. Driver/attenuator output spectrum at $+2$ dBm and -17 dBm average power.

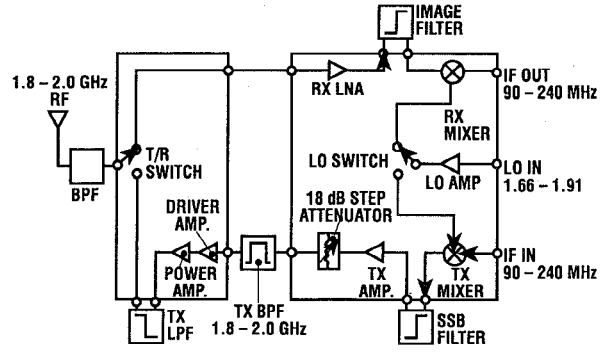

Fig. 26. RF chip set partition.

DQPSK signal modulated by a 9-bit psuedonoise sequence. Even with $+4$-dBm output power the sidelobe regrowth under drive is minimal and the ACI level at 600-kHz offset is better than 60 dBc as seen in Fig. 25. The system specification is 50 dBc. Following the driver amplifier is a 19-dB digital attenuator required for adaptive power control. This allows received power levels to be somewhat equalized at the base station when the portable station are at different distances from it. Fig. 25 shows the output spectrum in the high and low power states.

VI. Power Amplifier/Switch IC

The Power Amplifier and Transmit/Receive Switch completes the chip set. Fig. 26 shows the RF partition. The transmit band pass filter reduces the image and LO levels to 45 dBc required at the antenna. The main requirements of the power amplifier are:

1) Good adjacent channel distortion;
2) Low operational voltage 3 V; and
3) High power added efficiency

This requires optimization of the active device and the circuit design. Since the $\pi/4$ DQPSK signal to be amplified is continuously varying in amplitude and phase, any MESFET nonlinearity can distort the ideal Root Nyquist spectrum, causing sidelobe regrowth. Therefore it is not just the "hard" nonlinearities at the device knee or breakdown but also the soft nonlinearities such as gm $(V_{gs}, V_{ds}), C_{gs}\ (V_{gs}, V_{ds})\ R_{DS}$

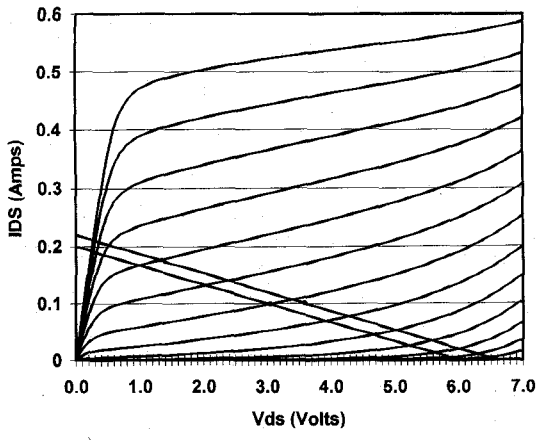

Fig. 27. I-V characteristics of 3-mm device (30 Ω load).

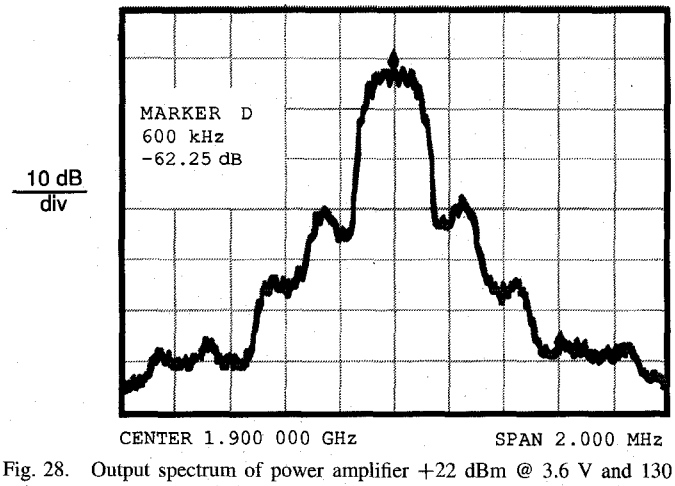

Fig. 28. Output spectrum of power amplifier +22 dBm @ 3.6 V and 130 mA.

(V_{gs}, V_{ds}) as the device swings over its load line. Thus linearity as a function of V_{gs}/V_{ds} is required for minimum side lobe regrowth. To optimize efficiency in the 3–3.6-V range it is desirable to have a device with the minimum "knee" voltage. A device with low pinch-off and knee voltage is thus more suitable than the traditional power device. By optimizing the load line and oversizing the device the "knee" voltage can be further reduced. Fig. 27 shows the I-V characteristics used in the final stage of the power amp design. A 3-mm device is chosen using a process with a buried Be P-layer. This helps to linearize gm at low currents. The pinch-off voltage is 1.2 V for this device the I_{DSS} is 520 mm. The quiescent bias of 100 mA (20% I_{DSS}) is chosen. Presenting a 30-Ω load line to this device allows for class AB operation. The real voltage swing is

$$V_{DD} - V_{\mathrm{knee}} = 3.0\text{–}0.5\ \mathrm{V} = 2.5\ \mathrm{V}.$$

The peak power is estimated at 23 dBm. The intrinsic linearity of gm (V_{gs}, V_{ds}) allows for minimum distortion on the load line. It is possible to simulate the effect of other device nonlinearities such as C_{gs} (V_{gs}, V_{ds}) on the output spectrum. This approach is lengthy and requires extreme precision in device models since 5th- and 7th-order nonlinearities need to be simulated. Our approach was to load pull the device to

TABLE III
POWER AMPLIFIER PERFORMANCE SUMMARY

Vdd1 / Vdd2	Pout (dBm)	ACI (dBc)	Pin (dBm)	Idd1/Idd2 (mA)	PAE (%)	Harmonics (dBc)
(4.8/5.8)	27	56	+5.8	212	39	41
4.0	23	60	1.8	138	34	48
3.6	22	61	1.1	130	34	43
3.5	22	59	1.2	130	35	42
3.4	22	57	1.7	125	37	34
3.0	21	60	1.0	110	38	42

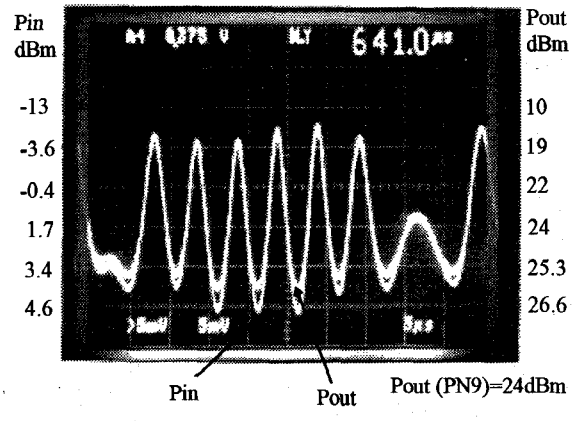

Fig. 29. Instantaneous power variation in the time domain.

achieve maximum efficiency band power under 60 dBc distortion levels using a $\pi/4$ DQPSK modulated source. Once the final stage FET periphery is established the two-stage design is optimized for maximum gain. The matching circuitry is realized using high Q inductors with a Q of 30. The available loss of the output matching circuits including plastic package losses is 0.5 dB. Fig. 28 shows the output spectrum of the final PA stage. It delivers +22 dBm of (π/4 DQPSK average power at 3.6 V bias with 60 dBc distortion. The overall efficiency is 34%. It is capable of delivering 21 dBm at 3 V thus allowing for 2-dB loss between the PA output and the antennae. Table III summarizes the output power and efficiency for various supply voltages. Fig. 29 shows instantaneous output power of the amplifier showing clearly compression of the peak output power.

The T/R switch uses a multigate design [5] to achieve low loss and high linearity. The insertion loss is 0.6 dB with an input intercept point of +48 dBm. Thus the switch causes no degradation in side lobe performance.

VII. MANUFACTURING THE CHIP SET

Many devices including LNA's, power amplifiers have been published recently [2], [5], [6]. This work represents the most highly integrated chip set available for PHS applications. The increased integration allows the RF portion of the phone to be realized with less board area allowing ultimately for a smaller handset. Fig. 30 shows the transceiver IC. All the functions are realized on a 3.5 mm^2 die. Fig. 31 shows the PA/switch IC which occupies 1.5 mm^2.

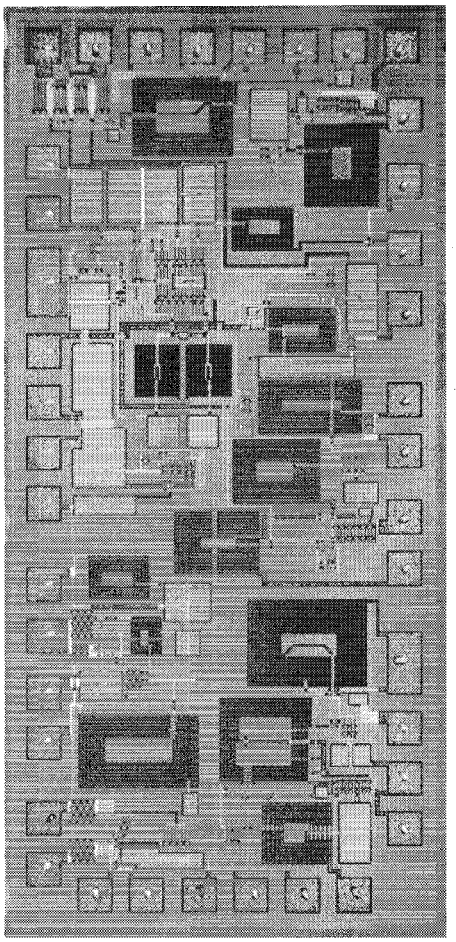

Fig. 30. Transceiver integrated circuit.

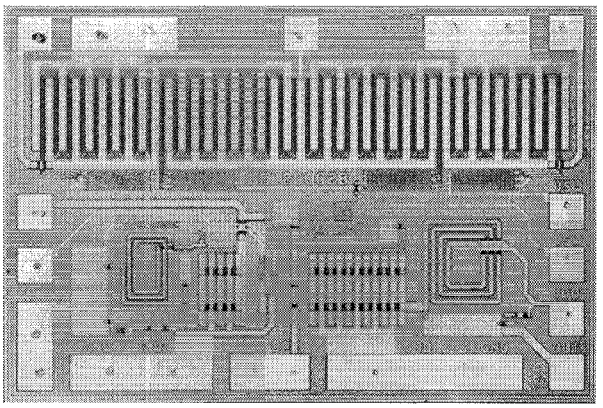

Fig. 31. Power amp/switch integrated circuit.

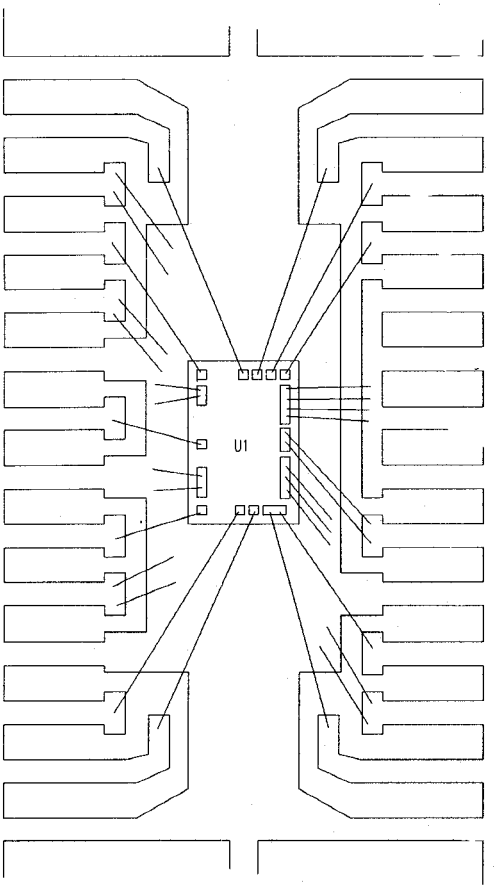

Fig. 32. Power amplifier switch assembly.

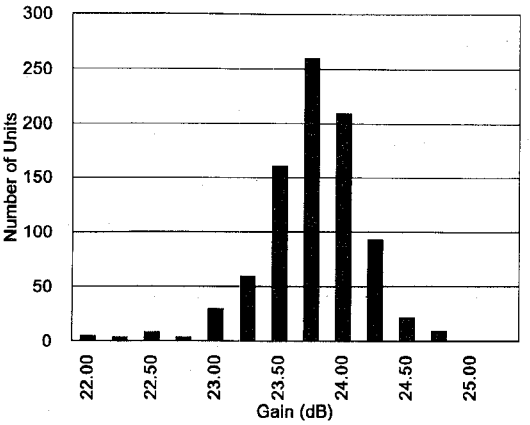

Fig. 33. Power amplifier gain statistic in production.

The chip set uses standard surface mount Shrink Small Outline (SSOP) Packages. Standard pick and place machines can be used in mass production. The packages are assembled using standard wire bonding and transfer molding techniques with a total cost of tens of cents. Fig. 32 shows the power amp and switch assembly. The use of standard packages allows for regular autohandlers to perform fully functional RF testing. Thus the complete chip set can be tested and the transceiver performance prediction before the PCB is assembled. Figs. 33 and 34 show the power amplifier gain and one dB compression point from a production lot of this power amplifier switch. Yields in excess of 90% have been achieved. As the manufacturing line matures the yield is expected to increase.

This chip set represents the standard in high volume highly integrated RFIC's currently available and is a crucial enabling technology for the PHS system. As the system is deployed in Japan usage of this kind of chip set is expected to be in the millions per year range. The PHS digital communications system is one of the major emerging global standards.

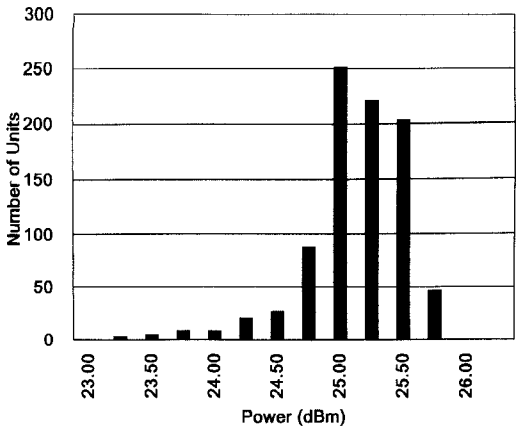

Fig. 34. Power amplifier one dB compression statistics in production.

REFERENCES

[1] Personal Handyphone System RCR Standard 28, Ver 1, Dec. 20, 1993.
[2] E. Heaney *et al.*, "Ultra low power low noise amplifiers for wireless communications," in *GaAs IC Symp.*, 1993, pp. 49–52.
[3] M. Nakatsugawa *et al.*, "An L-band ultra low power consumption monolithic low noise amplifier," in *GaAs IC Symp*, 1993, pp. 45–48.
[4] M. S. and J. M. Moniz, "A high performance GaAs MMIC up-conversion mixer for 2.45-GHz wireless spread spectrum communications" *IEEE MTT-S Euro. Topical Congress*, Nov. 2–5, 1994.
[5] F. McGrath, C. Kermarrec, C. Varmazis, and R. Pratt, "Multigate FET power switches," *Appl. Microwaves*, pp. 77–86, summer 1991
[6] T. Kunihisa, T. Yokoyama, H. Fujimoto, K. Ishida, H. Takehara, and O. Ishikawa, "High efficiency, low adjacent channel leakage GaAs power MMIC for digital cordless telephone," in *IEEE 1994 Microwave and Millimeter-Wave Circuits Symp.*, 1994.
[7] T. Yoshimasu, N. Tanba, and S. Hara, "An HBT linear power amplifier for 1.9-GHz personal communications," in *IEEE 1994 Microwave and Millimeter Wave Circuits Symp.*, 1994.

Finbarr McGrath was born in Cork, Ireland, on September 25, 1962. He received the B.Eng. (Electrical) degree from the National University of Ireland (Cork) in 1984 and the M.Eng.Sc. degree in 1986.

After graduating he worked at Pacific Monolothics Inc. (Sunnyvale, CA) from 1986–1989 developing broadband EW MMIC's and logarithmic amplifiers. From 1989 to the present he has worked at M/A-Com Microelectronics Division (Lowell, MA). He has developed novel high power switch and attenuator designs. He has also developed multifunction RFIC's for high volume commercial applications such as PHS and PCN chip sets. He is currently a Senior Principal Engineer at M/A-Com His main interests are circuit design and product development of innovative design solutions for emerging wireless products. He has coauthored over 20 papers and holds one patent.

Karen Jackson was born in Maryland on March 28, 1964. She received the B.S.E.E. from Clarkson University of Potsdam, NY, in 1986.

After graduating, she joined TRW's Communication Laboratory in Redondo Beach, CA, developing broadband MMIC's and hybrids for various receiver applications from 1986–1992. In 1992, she joined M/A-COM Microelectronics Division in Lowell, MA. She is currently a principal engineer working on the development of high volume commercial IC's.

Eugene Heaney received the B.E. and M.Eng.Sc. (Elec.) degrees from the National University of Ireland (Cork) in 1988 and 1990, respectively.

After graduating he joined Motorola's Cellular Infrastructure Group and worked in Arlington Heights. In 1991 he joined M/A-COM's Microelectronics Division. He has designed and developed multifunction RF IC's for high volume commercial applications in the 1.9–2.4-GHz range. He is currently a Senior Engineer designing RF IC products for next generation PCS applications. His interests include RF applications for digital communication systems and he is pursuing, part time, the Ph.D. degree in this area. He has co-authored eight papers.

Allan Douglas was born on November 19, 1959, in Bangor, ME. He received the B.S. degree in physics from Eastern Nazarene College (Quincy. MA) in 1982 and the M.S. degree in electrical engineering from Northeastern University in 1989.

After graduating he joined M/A-COM in the summer of 1982 where he developed test software for complex microwave assemblies. In 1985, he transfered to the subsystems design group and was responsible for the development of several receiver modules used in military systems. From 1992 to present, he has worked at the IC Products group as a Principal Engineer. In this capacity he has developed medium power MMIC amplifiers for high volume commercial applications such as PHS. His main interests are circuit design of amplifiers for the emerging wireless market.

William Fahey was born in Keene, NH, on May 14, 1961. He received his B.S.E.E. degree from Rensselaer Polytechnic Institute in Troy, NY, in May 1983.

After graduation he joined M/A-COM as a design engineer in the Solid State Components Division designing control components for defense programs. In 1988 he transferred to the Integrated Subsystems Division and worked on subsystems for military programs such as HARM, AMRAAM, and ASPJ. Since 1991 he has been with the IC Products Group of the Microelectronics Division designing GaAs MMICs for use in wireless communication markets. His current interests include automation techniques for high volume test, and cost reduction in MMIC manufacturing. He has authored or co-authored six papers.

Russell G. Pratt earned the B.S. degree at Westfield State College in 1976.

From 1978–1984 he served in the U.S. Navy as an electronic warfare technician. From 1984–1986 he was with M/A-COM in the Advanced Semiconductor Operations responsible for the study of GaAs passive and active devices. From 1986–1989 he was with Adams Russell Semiconductor Center engaged in the development of on-wafer noise and S parameter measurement systems. In 1989 he rejoined M/A-COM Microelectronics Division. Currently he is responsible for the characterization of multifunction MMIC's and devices destined for the wireless commercial market. He has co-authored three papers.

Ted Begnoche joined M/A-COM's GaAs MMIC development group in March, 1986. From 1986–1988 he worked in the fundamental studies group, characterizing low noise amplifier and passive component library structures. From 1988–1992 he was involved in characterizing components for a switch product line, including SPDT switches, attenuators, and phase shifters. From 1992 to the present Ted has been working on multifunction IC development, measuring transceivers, amplifiers, and modulators.